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DATA DEMODULATION USING AN ASYNCHRONOUS CLOCK

REFERENCE TO RELATED APPLICATION

This application claims priority to U.S. Provisional Patent Application Serial No. 60/405,914, filed August 26, 2002, the entire content of which is incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates generally to asynchronous data encoding and, in particular, to the use of an asynchronous clock to reliably demodulate a pulsewidth-modulated data stream.

BACKGROUND OF THE INVENTION

Many serial data protocols and mass storage devices rely upon asynchronous data encoding using multiple relative pulsewidths. Data is represented by two or more pulsewidths in a stream, usually with known fixed relative ratios. The base clock used is inferred by the data itself, rather than being separately provided.

Typical decoding methods for such data streams typically regenerate a clock frequency from the data stream, and count that clock per data state or transition to demodulate the data. This requisite clock regeneration step, however, introduces complexity and cost into systems with existing asynchronous clocks.

A need exists for a method to use an asynchronous clock to reliably demodulate a pulsewidth-modulated data stream.

SUMMARY OF THE INVENTION

This invention resides in a method and accompanying circuitry for asynchronous data demodulation using sorted pulsewidth measurement based on an asynchronous

clock. Lock-on of the data stream by such a system is accomplished by measured pulsewidth, rather than inferred frequency.

The method broadly comprises the steps of measuring a temporal aspect of the asynchronous clock, and locking onto the data stream in accordance with the measured periods.

In the preferred embodiment, the temporal aspect is a ratio of measured periods. Conveniently, a ratio of 2:1 may be used.

BRIEF DESCRIPTION OF THE DRAWING

Figure 1 is a block diagram showing a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to Figure 1, edge detector 101 receives as input serial data stream 100. For the purpose of this disclosure, the serial data stream 100 is assumed to convey binary information by differential time between state transitions, such that a binary '1' is indicated by a time period between two transitions double the time period used to indicate a binary '0'. Up-counter 103 receives its clock from free-running clock oscillator 104, the output frequency of which is preferably many times that of the highest frequency present in data stream 100.

At each transition of data stream 100, edge detector 101 outputs a very short duration transition pulse 105 to the clock input of latch 106, and delay 102. Delay 102 passes a delayed version of transition pulse 105 to the reset input of counter 103 and the clock input of Filter 111. The parallel output of counter 103 is latched by latch 106 upon receipt of each clock pulse. In that each transition pulse 105 latches the value of counter 103 and then resets counter 103 after the delay imposed by delay 102, the output 107 of latch 106 represents the width, in clock 104 pulses, between the previous two data

transitions of data stream 100. This width 107 is input to the 'A' input of comparator 114, divider 108, and the '0' input of multiplexer 109.

Divider 108 presents a value equal to half that of width 107 to the '1' input of multiplexer 109. The control input of multiplexer 109 is driven by the eventual output 115 of the demodulator, which indicates a binary '1' for a long inter-transition period and a binary '0' for a short period. Connected in this way, multiplexer 109 then outputs either the value of a detected short period or half the value of a detected long period, hence the minimum multiplexer measurement, to lowpass filter 111.

The divisor value of '2' for divider 108 reflects the ratio of incoming differential periods. The output of filter 111 is updated slightly after each data stream 100 transition by the pulse at its clock input noted earlier. This average minimum pulsewidth value is multiplied to 150 percent by multiplier 112 and presented to the 'B' (reference) input of comparator 114. The multiplicand '1.5' for multiplier 112 is chosen to represent the median of the ratio of incoming differential periods.

Comparator 114 compares the incoming period measurement 107 with this reference average median period to determine if the incoming period is closer to the average minimum period or twice the average minimum period. The binary result 115 of comparator 114 then represents the demodulated value of incoming data stream 100.

Note that demodulation is effected by ratios of measured periods, thus obviating any synchronous clocks or frequency tracking. Although a ratio of 2:1 is illustrated, it will apparent to one of skill that other ratios and/or number of modulation states will benefit as well from the invention described herein.

I claim: